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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/763,693	01/23/2004	Nicholas Holian	200312299-1	7674

22879 7590 08/22/2007

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EXAMINER	
WILSON, YOLANDA L	
ART UNIT	**PAPER NUMBER**
2113	

MAIL DATE	DELIVERY MODE
08/22/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/763,693	HOLIAN ET AL.	
	Examiner	Art Unit	
	Yolanda L. Wilson	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 June 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-17 and 20-22* is/are rejected.

7)☒ Claim(s) *18 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1,3-8 are rejected under 35 U.S.C. 102(b) as being anticipated by IBM Disclosure (NB9406439). As per claim 1, IBM Disclosure discloses a plurality of memory circuits; a plurality of data lines coupled to the plurality of memory circuits, the plurality of data lines transfer data to and from the plurality of memory circuits; a switching device coupled to at least one of the plurality of data lines, the switching device attached to the outer surface of one of the plurality of memory circuits; and wherein the switching device selectively operates to simulate a hardware error on at least one of the plurality of data lines based on an input signal from a control logic external to the memory module on page 1. The switching device is the memory interposer. Control logic is the fault injection software from the host system.

3. As per claim 3, IBM Disclosure discloses wherein the switching device electrically floats the at least one of the plurality of data lines on page 1, "Address inputs...inverted."

4. As per claim 4, IBM Disclosure discloses wherein the switching device drives the at least one of the plurality of data lines to a high voltage level on page 1, "Address inputs...inverted."

5. As per claim 5, IBM Disclosure discloses wherein the switching device drives the at least one of the plurality of data lines to a low voltage level on page 1, "Address inputs...inverted."

6. As per claim 6, IBM Disclosure discloses receiving a request by a control logic to simulate a hardware error on a data line of a memory module; and simulating the hardware error on the data line by a switching unit attached to an outer surface of one of a plurality of memory circuits on the memory module on page 1. The switching device is the memory interposer. Control logic is the fault injection software from the host system.

7. As per claim 7, Abramov et al. discloses sending instructions to inject the error to the control logic from an application executing in a computer system coupled to the memory module on page 1.

8. As per claim 8, Abramov et al. discloses sending the instructions on a communication bus on page 1.

9. Claims 20-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Abramov et al. (USPN 6327676B1).

10. As per claim 20, Abramov et al. discloses a plurality of means for storing data, wherein at least one of the means for storing data is integrated with a means for driving a simulated hardware error; a plurality of means for transferring data to and from the plurality of means for storing data; and wherein the means for driving is operable to one of drive a voltage and electrically float at least one of the plurality of means for

transferring data in column 4, lines 28-35 and in column 8, line 66 – column 9, line 10. The switching device is the test equipment.

11. As per claim 21, Abramov et al. discloses wherein the means for driving applies a voltage based on a request from a software application in column 4, lines 28-35 and in column 8, line 66 – column 9, line 10.

12. As per claim 22, Abramov et al. discloses wherein the means for driving further comprises a means for interfacing with a communications bus in column 4, lines 28-35 and in column 8, line 66 – column 9, line 10.

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over IBM Disclosure in view of Webopedia. As per claim 9, IBM Disclosure fails to explicitly state sending the instructions on an inter-integrated circuits (I2C) communications bus.

Webopedia discloses this limitation on page 1.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to send the instructions on an inter-integrated circuits (I2C) communications bus. A person of ordinary skill in the art would have been motivated to

send the instructions on an inter-integrated circuits (I2C) communications bus because the I2C bus is used to connect devices to be used in a computer system.

15. Claims 10-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over IBM Disclosure in view of IBM Disclosure (NN9210142).

16. As per claim 10, IBM Disclosure fails to explicitly state wherein simulating the hardware error comprises driving a high voltage on the data line in the memory module to simulate a stuck-at-1 hardware error.

IBM Disclosure (NN9210142) discloses this limitation on page 1.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have simulating the hardware error comprises driving a high voltage on the data line in the memory module to simulate a stuck-at-1 hardware error. A person of ordinary skill in the art would have been motivated to have simulating the hardware error comprises driving a high voltage on the data line in the memory module to simulate a stuck-at-1 hardware error because simulating this type of error determines whether or not the system can detect this type of error.

17. As per claim 11, IBM Disclosure fails to explicitly state wherein simulating the hardware error comprises electrically floating a data line in the memory module to simulate a stuck-open hardware error.

IBM Disclosure (NN9210142) discloses this limitation on page 1.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have simulating the hardware error comprises electrically floating a data line in the memory module to simulate a stuck-open hardware

error. A person of ordinary skill in the art would have been motivated to have simulating the hardware error comprises electrically floating a data line in the memory module to simulate a stuck-open hardware error because simulating this type of error determines whether or not the system can detect this type of error.

18. As per claim 12, IBM Disclosure fails to explicitly state wherein simulating the hardware error comprises electrically grounding the data line in the memory module to simulate a stuck-at-0 fault.

IBM Disclosure (NN9210142) discloses this limitation on page 1.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have simulating the hardware error comprises electrically grounding the data line in the memory module to simulate a stuck-at-0 fault. A person of ordinary skill in the art would have been motivated to have simulating the hardware error comprises electrically grounding the data line in the memory module to simulate a stuck-at-0 fault because simulating this type of error determines whether or not the system can detect this type of error.

19. As per claim 13, IBM Disclosure fails to explicitly state wherein simulating the hardware error comprises simulating a hardware error for a predetermined amount of time, the simulated hardware error being one selected from the group consisting of a stuck-at-1 hardware error, a stuck-at-0 hardware error, and a stuck-open hardware error.

IBM Disclosure (NN9210142) discloses this limitation on page 1.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have simulating the hardware error comprises simulating a hardware error for a predetermined amount of time, the simulated hardware error being one selected from the group consisting of a stuck-at-1 hardware error, a stuck-at-0 hardware error, and a stuck-open hardware error. A person of ordinary skill in the art would have been motivated to have simulating the hardware error comprises simulating a hardware error for a predetermined amount of time, the simulated hardware error being one selected from the group consisting of a stuck-at-1 hardware error, a stuck-at-0 hardware error, and a stuck-open hardware error because simulating this type of error determines whether or not the system can detect this type of error.

20. Claims 14-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Berry Jr. et al. in view of IBM Disclosure (NB9406439).

21. As per claim 14, Berry Jr. et al. discloses a central processing unit (CPU); a memory coupled to the CPU; and control logic coupled to the memory and to the CPU, the control logic operable by the CPU to enable operation of a switching device coupled to a memory module to simulate a hardware error in the memory module; wherein the switching device and the memory module are both physically located inside the system on page 1, paragraph 0011 and page 5, paragraph 0048.

Berry Jr. fails to explicitly state wherein the switching device is attached to an outer surface of one of the plurality of memory circuits.

IBM Disclosure (NB 9406439) discloses this limitation on page 1, '...The SIMM target for fault injection plugs directly into the memory interposer...'.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the switching device is attached to an outer surface of one of the plurality of memory circuits. A person of ordinary skill in the art would have been motivated to have the switching device is attached to an outer surface of one of the plurality of memory circuits because having the switching device attached to an outer surface still provides the same functionality of being able to simulate errors in the memory module.

22. As per claim 15, Berry Jr. et al. discloses wherein the switching device is operable to apply a high voltage level to a data line in the memory module.

IBM Disclosure (NB 9406439) discloses this limitation on page 1, "Address inputs...inverted."

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the switching device is operable to apply a high voltage level to a data line in the memory module. A person of ordinary skill in the art would have been motivated to have the switching device is operable to apply a high voltage level to a data line in the memory module because simulating this type of error determines whether or not the system can detect this type of error.

23. As per claim 16, Berry Jr. et al. fails to explicitly state wherein the switching device is operable to apply a low voltage level to a data line in the memory module.

IBM Disclosure (NB 9406439) discloses this limitation on page 1, "Address inputs...inverted."

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the switching device is operable to apply a low voltage level to a data line in the memory module. A person of ordinary skill in the art would have been motivated to have the switching device is operable to apply a low voltage level to a data line in the memory module because simulating this type of error determines whether or not the system can detect this type of error.

24. As per claim 17, Berry Jr. et al. fails to explicitly state wherein the switching device electrically floats a data line in the memory module.

IBM Disclosure (NB 9406439) discloses this limitation on page 1, "Address inputs...inverted."

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the switching device electrically floats a data line in the memory module. A person of ordinary skill in the art would have been motivated to have the switching device electrically floats a data line in the memory module because simulating this type of error determines whether or not the system can detect this type of error.

Claim Objections

25. Claims 18,19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

26. Applicant's arguments filed 06/08/2007 have been fully considered but they are not persuasive. Applicant argues on 7, under the IBM '439 Anticipation Rejections Section, '...Applicants respectfully submit that such contact cannot be reasonably interpreted to encompass attaching a switching device to an outer surface of a memory circuit...does not teach or even suggest attaching the switch to an outer surface of a memory circuit within the memory module...'

27. Examiner respectfully disagrees. As disclosed in the IBM '439 reference, 'The SIMM target for fault injection plugs directly into the memory interposer'; therefore, the switching device and the memory circuit are connected to one another by way of the outer surface.

28. Applicants arguments under The Berry Anticipation Rejections are moot in view of the '439 reference used to reject the newly added limitation in claim 14. Rationale for the 103 obviousness was made using the KSR Supreme Court decision.

Conclusion

29. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yolanda L. Wilson whose telephone number is (571) 272-3653. The examiner can normally be reached on M-F (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Yolanda L Wilson
Primary Examiner
Art Unit 2113